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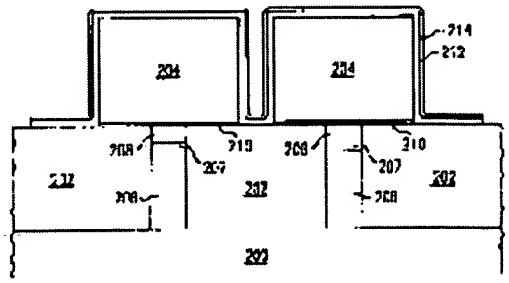
(54) INTEGRATED CIRCUIT CAPACITOR AND MEMORY

(57)Abstract:

PROBLEM TO BE SOLVED: To strengthen bonding of capacitor bottom electrodes to interlayer insulators and to raise the conductivity of the bottom electrodes to conductive plugs by a method wherein the capacitor bottom electrodes of a memory circuit comprising a memory cell are bonded to the interlayer insulators making barrier body layers, the conductive plugs and the like interpose between the side surfaces of the interlayer insulators and making conductive bonding accelerating



layers interpose between the bottom electrodes and the upper surfaces of the interlayer insulators.

SOLUTION: Two capacitor bottom electrodes 204, which have a charge storage layer or a capacitor insulator 212 and a top electrode 214, of a memory circuit comprising a memory cell are bonded on a silicon substrate 200 via silicon dioxide interlayer insulators 202 and barrier body layers 208 consisting of a Ti-Al-N layer. The insulators 202 are separated from each other by the layers 208, silicide layers 207 consisting of a TiSi2 layer and conductive plugs 206, which are laminated. The electrodes 204 consist of a platinum layer of a thickness of about 350 nm or the like, are formed into a rectangular shape and conductive bonding accelerating layers 210 consisting of a Ti-N layer or the like are respectively interposed between the electrodes 204 and the insulators 202 under the lower surfaces of the electrodes 204. Thereby, a bonding of the electrodes 204 to the insulators 205 and the conductivity of the electrodes 204 to the plugs are enhanced.

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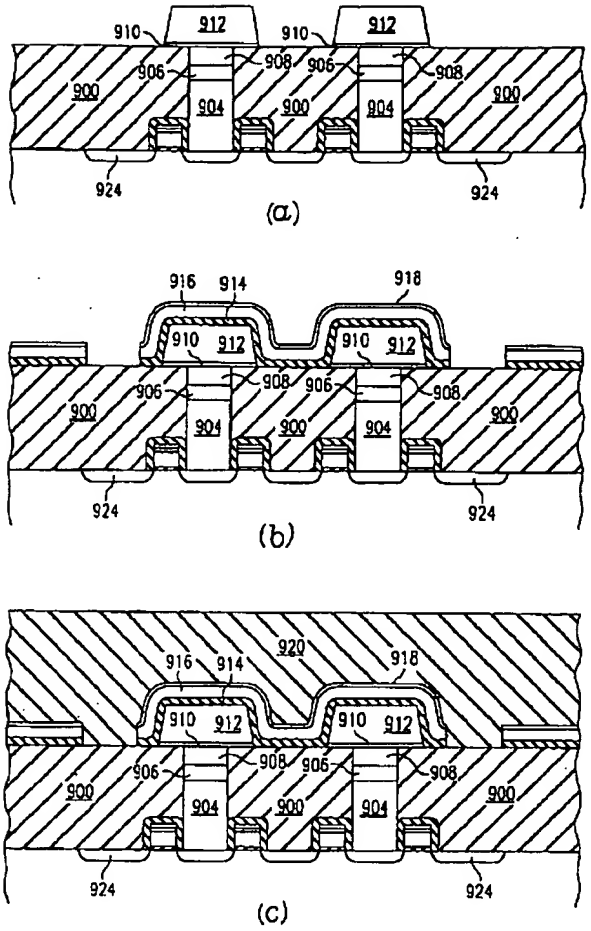

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a detail further about an electron device at a semiconductor integrated circuit capacitor and its manufacture approach.
[0002]
[Description of the Prior Art] Buildup of the want to semiconductor memory and the need for contention are imminent, and one transistor and the integrated-circuit dynamic random access memory (DRAM) of the one-layer high density based on the memory cell of one capacitor are needed. However, making small the dimension of standard oxidation and the capacitor of a silicon nitride insulator (dielectric) has the trouble including the amount of charges accumulated into a cel decreasing. Therefore, the insulator of the alternative with a bigger dielectric constant than oxidation and silicon nitride is investigated. "Insulator ingredient of Ta2 O5 capacitor of Gigabit DRAM" IEEE IEDM Tech.Dig.5.1.1 besides an Aussie (1995 year) Tantalum pentoxide which was indicated (a dielectric constant is about 25 to the dielectric constant 7 [about] of silicon nitride), "Formation of Pb(Zr, Ti) O3 thin film on electrode containing IrO2" 65 Appl.Phys.Lett.1522 besides Nakamura (1994) Were indicated. The titanic-acid lead zirconate which is a ferroelectric and supports a non-volatile charge storage (PZT) (a dielectric constant is about 1000), Jean (Jiang) Other "electrode technical" VLSI Tech.Symp.26 with the new non-volatile ferroelectric (SrBi2 Ta 2O9) memory of high density (1996 year) Indicated tantalic acid bismuth strontium (similarly ferroelectric), And "ECR MOCVD (Ba, Sr) TiO3 based on laminating capacitor technique of having RuO2/Ru/TiN/TiSix are recording node of DRAM of gigabit magnitude" IEEE IEDM Tech.Dig.5.3.1 besides YAMAMICHI (1995), "Laminating capacitor technical" IEEE IEDMTech.Dig.5.2.1 with new 1-gigabit DRAM which has the CVD-(Ba, Sr) TiO3 thin film on the thick are recording node of Ru besides YUUKI (1995), And "laminating capacitor [which has the TiO (Ba, Sr)3 insulator and Pt electrode of DRAM of a 1 gigabit consistency] technical" VLSI Tech.Symp.24 besides Park (1996 year) Indicated barium titanate strontium (a dielectric constant is about 500), Various insulator ingredients can be used. Furthermore, DITSU (Dietz) (electrodes on strontium titanate, such as Pt, Pd, and Au, are indicated) Other "electrode effect [to the charge transfer through SrTiO3 thin film] (influence)" 78 J.Appl.Phys.6113 (1995 year), And please refer to the United States patent number No. (PZT and barium titanate) 5,003,428, the United States patent number No. 5,418,388 (BST, SrTiO3, PZT, etc.), and the United States patent number No. (thin Pt on BST) 5,566,045.
[0003] The deposit of the insulator of these alternatives is typically carried out in an elevated temperature and an oxidizing atmosphere. Consequently, it is stable to oxygen (oxygen-stable). Platinum, ruthenium oxide, etc. are used as a pars-basilaris-ossis-occipitalis electrode material. However, since a silicide is formed easily and it is further spread quickly to a platinum grain boundary when touching silicon directly, platinum is not a good obstruction object over oxygen. In the United States patent number No. 5,504,041, the summer felt uses the conductive nitride obstruction body whorl for the bottom of a platinum electrode in order not to make the lower layer which is easy to oxidize

diffuse oxygen. Another trouble about a platinum electrode is that adhesion of the platinum to diacidized silicon, silicon nitride, and other common layer insulation object ingredients is weak. The structure of the platinum which patterning was carried out and was etched tends to exfoliate in process [consecutiveness] (debond). The United States patent number No. 5,489,548, 5,609,927, and 5,612,574 have proposed using a glue line, in order to avoid that a platinum electrode exfoliates.
[0004] Some of insulator of these alternatives, for example, PZT, BST(s), and SBT(s), is a ferroelectric, therefore they can be used as an are recording object of ferroelectric nonvolatile RAM (FRAM). If it removes being used to the charge in an ingredient showing the content of data of the cel of DRAM in order that polarization (polarization) of a ferroelectric ingredient may show the content of data of the cel of FRAM, the FRAM cel is similar to the DRAM cel. Although polarization of an ingredient is nonvolatile, the charge in DRAM is dissipated.
[0005]
[The means and operation] for attaining a technical problem The memory circuit containing a memory cell is indicated according to one example of this invention. A memory cell contains the top electrode in contact with the accumulation layer in contact with the 2nd front face of the pars-basilaris-ossis-occipitalis electrode which has a conductive adhesion acceleration layer on the 1st front face, and a pars-basilaris-ossis-occipitalis electrode, and an accumulation layer. A memory cell contains further the transistor containing the 1st and 2nd terminals and word line control terminals, and the bit line combined with said 1st transistor terminal. A pars-basilaris-ossis-occipitalis electrode is combined with the 2nd transistor terminal by the plug including the obstruction object which adjoins an adhesion acceleration layer, and this obstruction object is thicker than an adhesion acceleration layer. The advantage of this new concept is being built so that a platinum electrode's may paste a layer insulation object, and being able to prevent a concave oxidation obstruction object from oxidizing by the obstruction object / electrode interface.
[0006] According to another example of this invention, it is a certain configuration (feature) to the platinum layer which is on the 2nd ingredient, without etching the 2nd ingredient substantially. The approach of etching is indicated. This approach forms an adhesion acceleration layer between a platinum layer and the 2nd ingredient, forms a hard surface mask blank layer on a platinum layer, according to the dimension of a request of that configuration, carries out patterning of the hard surface mask blank layer, etches it, etches the part of the platinum layer which is not covered with a hard surface mask blank layer, and includes the process which suspends etching on an adhesion acceleration layer. In the further example, an adhesion acceleration layer and a hard surface mask blank layer are Ti-aluminum-N containing at least 1% of aluminum.
[0007] The approach of etching platinum is indicated according to other examples of this invention. This approach forms a Ti-aluminum-N hard surface mask blank layer on platinum, carries out patterning of the Ti-aluminum-N hard surface mask blank layer, etches it by the chlorine content etching agent (chlorine-bearing etchant), forms a desired pattern, and includes the process which etches platinum by the oxygen content (oxygen-bearing) etching agent further. The advantage of this new concept is that the platinum for which patterning and etching were difficult may be etched into a detailed configuration and a steep side-attachment-wall profile.
[0008] According to another desirable example of this invention, the high beer etching process of a selection ratio is indicated. This process forms the dirty stop layer of the ingredient chosen from the group who consists of Ti-aluminum, Ti-aluminum-N, Ta-aluminum, aluminum-N, Ti-aluminum/Ti-N, Ti-aluminum-N/Ti-N, Ta-aluminum/Ti-N, and Ti-aluminum/Ti-aluminum-N, forms an insulator layer on a dirty stop layer, and includes the process which etches an insulator layer by the fluorine content etching agent further. The advantage of this new concept is that the ingredient formed (featured) has high etch selectivity compared with the layer insulation object usually used. Therefore, it may be carried out, without etching through a dirty stop layer, when the beer whose beer etching process containing long over etching is two from which the depth differs greatly is etched at the same process. In addition to the ingredient formed functioning as a very effective dirty stop layer, especially etching, such as platinum, is also good hard surface mask blank ingredients for a difficult ingredient.

[0009]
[Example] He can understand the above-mentioned property of this invention still better by reading the below-mentioned detailed explanation with reference to an attached drawing.
[0010] a general view -- adhesion of the electrode to an adjoining ingredient is promoted and a desirable example offers the capacitor which has an effective obstruction object over oxidation. Another example covers the approach of forming the electrode which has a steep side-attachment-wall profile and has an effective obstruction object over oxidation and a reaction, and an electrode, and offers the approach of making easy the following process process. A desirable example can be used in DRAM, FRAM, and the integrated circuit of other classes.
[0011] Drawing 1 (a) and 1 (b) show the electrode of two advanced technology with a sectional view. This structure is built on the semi-conductor substrate 100. A capacitor keeps distance typical from a substrate front face with the layer insulation object 102 in consideration of a near transistor, a bit line, etc. a substrate front face. The connection between an electrode 104 and a substrate front face is accomplished by the conductive plug 106. Reaction/oxidation obstruction object 108 is arranged between the electrode which consists of platinum typically, and the plug which consists of polish recon typically. the case where there is no obstruction object 108 -- about 400 degrees C -- between a platinum electrode and polish recon plugs -- silicification -- platinum is formed. the diacid-ized silicon which is an insulating material when there is oxygen -- silicification -- it is formed from platinum and the conductivity of the combination of a plug / obstruction object / electrode is influenced.
[0012] The layer insulation object 102 is diacid-ized silicon or silicon nitride typically. Any of these ingredients do not paste up platinum well. Although it is better than the adhesive property of platinum, it is not enough for the configuration which can permit the yield and by which patterning was carried out minutely, and the adhesive property of a ruthenium and iridium is adhesion loss (adhesion loss). It accumulates and there is no long-term dependability. The approach of the advanced technology of improving the adhesive property over an insulator is a thin interlayer's activity. The summer felt proposed titanium, the tantalum, and the ruthenium as a thin adhesion acceleration layer by the United States patent number No. 5,612,574. In the structure of the advanced technology shown in drawing 1 (a), since the obstruction body whorl 108 is between the layer insulation object 102 and the platinum pars-basilaris-ossis-occipitalis electrode 104 over the whole electrode, a permissible adhesive property is offered. Such approach is proposed in the United States patent number No. 5,504,041. The part to which, as for the fault of this approach, the obstruction body whorl 108 was exposed is easy to oxidize while carrying out the deposit of a high dielectric constant or the capacitor insulator (not shown) of a ferroelectric on an electrode 104. Although the structure of drawing 1 (b) avoids the problem of oxidation of this obstruction object, the adhesive property between the pars-basilaris-ossis-occipitalis electrode 104 and the layer insulation object 102 is weak.
[0013] Structure drawing 2 shows the capacitor of a desirable example with a sectional view. Two of said capacitors are shown that it clarifies relation of the adjoining pars-basilaris-ossis-occipitalis electrode 204. A substrate 200 is a semiconductor material and is silicon or silicon-on-insulator (silicon-on-insulator) preferably. Although the layer insulation object 202 is diacid-ized silicon (SiO2) preferably In an alternative example, it is Si3 N4, Si-N, Si-O, Si-O-N, and SiO2. And that by which the ingredient enumerated before was doped, TiO2, aluminum 2O3, ZrO2, MgO and Ta 2O5, V2 O5, Y2 O3, and Nb 2O5 It is contained. Notice a layer insulation object about that your may be the combination of the multiplex layer of another ingredient, or an above-mentioned ingredient. Notice the notation "A-B-C", such as furthermore, "Si-O-N", about it being shown that the ingredient exists with the various configurations of Elements A, B, and C. The thickness of a layer insulation object is chosen so that the structures which are downward, such as a transistor gate and the bit line structure (not shown), may be clarified, and typical thickness is about 200nm. The conductive plug 206 is silicon by which the Lynn dope was carried out preferably, and is about 100nm in width of face. In the alternative example of a plug ingredient, they are Ti-N, Ti-aluminum-N, W and Cu, aluminum-Cu, aluminum and Ti, Ti-Si-N, W-Si-N, Ti-Si, Ta-Si, W-Si, and TiSi2. It is contained. The obstruction body whorl 208 is Ti-aluminum-N preferably, the configuration is the range between Ti-N and (Ti0.5aluminum0.5) -N, and it is desirable

that it is (Ti0.75aluminum0.25)-N. Although the thickness of an obstruction object may be the range between 10nm and 100nm, the desirable range is for 20nm and 50nm. For the alternative example of an obstruction object ingredient, Ta-N, Ta-aluminum-N, Ti-Si-N, W-Si-N, Ru-N, W-N, Ru-aluminum-N, Ru-Si-N, Cr-N, Cr-aluminum-N, Mo-N, Mo-aluminum-N, Mo-Si-N, V-N, V-Si-N, V-aluminum-N, Hf-N, Hf-aluminum-N, A 3 yuan nitride (or further pluralism) (for example, Ta-Si-N, Ta-B-N, Ti-B-N), Zr-N, Y-N, Sc-N, La-N, nitrogen starvation aluminum-N, doped aluminum-N, Mg-N, calcium-N, Sr-N, Ba-N, and an above-mentioned alloy are contained. A noble-metals insulating material alloy, for example, Pt-Si-N, Pd-Si-O, Pd-B- (O, N), Pd-aluminum-N, Ru-Si- (O, N), Ir-Si-O, Re-Si-N, Rh-aluminum-O, Au-Si-N, and Ag-Si-N are contained in another alternative example of an obstruction object ingredient. Notice an obstruction body whorl about that the combination of the multiplex layer of another ingredient or an above-mentioned ingredient may be included. the conductive plug 206 and the obstruction body whorl 208 -- silicide layer 207 2, for example, TiSi, etc. -- it may dissociate.

[0014] The pars-basilaris-ossis-occipitalis electrode 204 is platinum which has the thickness of the range of about 30 to 1000nm preferably, and it is desirable that it is about 350nm. The base of the electrode of DRAM is a rectangle with a dimension of fx3f, and f is a critical size (namely, lower limit of an electrode) here. The range of the critical size of DRAM is about 0.05 to 1 micrometer, and it is about 0.16 micrometers preferably. On the other hand, the electrode of FRAM has a critical size typically smaller than about 1 micrometer or it. Ru, Rh, Pd, Re, Ir and the alloy of the ingredient of above-mentioned arbitration, Pt-O, RuO2, Ru-O, Rh-O, Pd-O, IrO2, Ir-O, Re-O and an above-mentioned alloy (an oxygen content alloy, for example, Pt-Rh-O), SrRuO3, Sn-O, and In-Sn-O are contained in the alternate material of a pars-basilaris-ossis-occipitalis electrode. Notice a pars-basilaris-ossis-occipitalis electrode about that the combination of the multiplex layer of another ingredient or an above-mentioned ingredient may be included. It is desirable that the adhesion acceleration layer 210 is conductivity and the configuration is Ti-aluminum-N of the range between Ti-N and (Ti0.5 aluminum0.5) -N, and it is -(Ti0.75aluminum0.25) N preferably. An adhesion acceleration layer has the thickness of the range between about 0.2nm and 10nm, and desirable thickness is about 3nm. The adhesion acceleration layer 210 is not continuing between two capacitors in order to offer the electrical isolation (isolation) of the pars-basilaris-ossis-occipitalis electrode 204. For the alternative example of the ingredient of an adhesion acceleration layer, Ta-aluminum-N, Ti-Si-N, W-Si-N, W-N, W-Si-N, Cr-N, Cr-aluminum-N, Mo-N, Mo-aluminum-N, Mo-Si-N, Si-N, Si, germanium, V, V-N, V-Si-N, V-aluminum-N, Ti-Si, Ta-Si, W-Si, Mo-Si, Cr-Si, Pt-Si, W, Ta, Ti, Sn, Ru, In, Os, Rh, Ir, a 3 yuan nitride (or further pluralism) For example, (Ta-Si-N, Ta-B-N, Ti-B-N), Zr-N, Y-N, Sc-N, La-N, nitrogen starvation aluminum-N, doped aluminum-N, Mg-N, calcium-N, Sr-N, Ba-N, and an above-mentioned alloy are contained. A noble-metals insulating material alloy, for example, Pt-Si-N, Pd-Si-O, Pd-B- (O, N), Pd-aluminum-N, Ru-Si-(O, N), Ir-Si-O, Re-Si-N, Rh-aluminum-O, Au-Si-N, and Ag-Si-N are contained in another alternative example of the ingredient of an adhesion acceleration layer. Notice an adhesion acceleration layer about that the combination of the multiplex layer of another ingredient or an above-mentioned ingredient may be included.

[0015] The thin film of silicon may also function as an adhesion acceleration layer. During consecutive heat treatment, this layer reacts with a pars-basilaris-ossis-occipitalis electrode, and forms the very thin silicide layer which may function as an adhesion acceleration layer later. the amount of the silicide formed since the amount of silicon is restricted based on the thickness by which a deposit is carried out -- few -- self -- it is restrictive (self-limiting) it is . This differs from the case where the obstruction object between a polish recon plug and a pars-basilaris-ossis-occipitalis electrode suffers a loss (fail). in that case, a reaction -- self -- it leads to a device defect that it is not restrictive and fatal. Thin SiO2 Since a layer may be formed by the self-inactivation (self-passivating) method on the exposed small field, the thin silicide formed in the base of an electrode also has oxidation resistance of enough. The effect which this has on the whole engine performance of a capacitor is small because of the thickness of this layer.

[0016] Preferably, although a charge accumulation layer or the capacitor insulator 212 is Ba-Sr-Ti-O (Ba, Sr) (TiO3) which has the thickness of the range of about 3 to 150nm, it is desirable that it is the thickness of about 25nm. In the alternative example of an accumulation layer ingredient, they are Ta

2O5, PZT, and Ba1-x Srx Ti1-y Zry O3 (). Or more generally they are BSZT and Pb1-x Lax Ti1-y Zry O3 (). Or more generally, PLZT and Bi2 A1-x Bx O3x-3 (or a perovskite group's ingredient more generally stratified) are contained, A is Ba, Sr, calcium, Pb, or Ga, and B is Ti, Ta, Zr, or Nb here. Generally, a desirable accumulation layer ingredient has a larger dielectric constant than 50 or it. The top electrode 214 is platinum which has the thickness of the range of 10 to 100nm preferably, and it is desirable that it is the thickness of about 25nm. In addition to what was enumerated before, Ti-N, Ti-aluminum-N, Ta-N, Ta-aluminum-N, W-N, W-aluminum-N, Cr-N, Cr-aluminum-N, Ru-N, Ru-aluminum-N, Mo-N, Mo-aluminum-N, V-N, V-aluminum-N, Hf-N, and Hf-aluminum-N are contained in the alternate material of a top electrode for pars-basilaris-ossis-occipitalis electrodes.

[0017] One pair of capacitors are again shown so that drawing 3 may show the capacitor of the 2nd desirable example and relation between adjoining capacitors may be clarified. Patterning of the configuration of a pars-basilaris-ossis-occipitalis electrode material with the detailed advantage of this cellular structure object and etching are not needing. Rather, patterning and etching are about the insulator layer between capacitors. Metaled detailed patterning causes the problem of a reflection factor (reflectivity), and especially etching of platinum is dramatically difficult. Furthermore, since the activity of a pars-basilaris-ossis-occipitalis electrode material is made more as for this structure to small quantity, it can serve as economization of ingredient cost. Another advantage of the cel of the 2nd desirable example is not removing the insulator between nodes. This structure is free standing (free-standing). Compared with the cel of the crown mold which has a metal, it is physically stable.

[0018] a capacitor -- desirable -- SiO2 it is -- it is formed in the trench of the insulator ingredient 316 between capacitors. The "base" of a trench is similar to the electrode of a laminating mold (namely, fx3f). The width of face of the insulator between capacitors is about f which is a critical-value dimension. The thickness of the insulator between capacitors is about 350nm. Si3 N4, Si-O, Si-N, Si-O-N, and the thing by which the **** was doped are contained in the alternative example of an insulator. In order that the structure of drawing 3 may offer the capacitor field which increased, there is much more much capacity per same physical space. Although, as for the adhesion acceleration layer 310, the pars-basilaris-ossis-occipitalis electrode 304 ensures not being removed by consecutive down stream processing along with a trench, in order to maintain the electrical isolation of the pars-basilaris-ossis-occipitalis electrode 304, the layer 310 is not continuing between capacitors. The pars-basilaris-ossis-occipitalis electrode 304 is thinner than the thing of the example shown in drawing 2 . The range of the thickness is about 10 to 50nm, and it is desirable that it is about 20nm. In respect of others, the structure of drawing 3 is similar with what was shown in drawing 2 , and contains the layer insulation body whorl 302 formed on a substrate 300. The pars-basilaris-ossis-occipitalis electrode 304 contacts a substrate 300 through the conductive adhesion acceleration layer 310, the oxidation obstruction object 308, the silicide layer 307, and a plug 306. The pars-basilaris-ossis-occipitalis electrode 304 is the capacitor insulator 312, and then is covered with the top electrode 314. Please refer to the 1st above-mentioned desirable example about selection and the alternative example of an ingredient.

[0019] Drawing 4 is the same as that of what showed the capacitor of the 3rd desirable example, and showed it to drawing 3 when removing having not become depressed as the obstruction object 408 is shown in drawing 3 . The deposit of an obstruction object and the adhesion acceleration layer 410 may be carried out at the single process which has the process which can control independently the coat of a side attachment wall and a pars basilaris ossis occipitalis. An example of such a process is ionization sputtering and is performed by heating and (thermalize) ionizing the flux (flux) (these atoms being neutrality usually electrically) which comes out of the target which carries out a spatter and by which the spatter was carried out. This puts a coil on a chamber and accomplishes it by exciting it with RF power. the auto-bias which produces the ionized spatter atom between a wafer and the plasma -- or the bias supplied by the external power on a wafer accelerates to a wafer. This acceleration changes the flux distribution to a wafer, and directivity becomes large rather than the usual sputtering source. By adjusting ionization and a bias property, more [or] fewer partes basilaris ossis occipitalis and a side-attachment-wall coat can be obtained like a request. In this process, a pars-basilaris-ossis-occipitalis coat serves as good approach against a trench cel desirable [it is larger than the coat of a side attachment

wall, and] in order that it may raise the engine performance of an obstruction object that the pars-basilaris-ossis-occipitalis film is thicker than the film of a side attachment wall typically. Furthermore, when an obstruction object and an adhesion acceleration layer consist of same ingredients, this serves as an advantage in this example.

[0020] Drawing 5 shows the crown cel capacitor of the 4th desirable example. This structure is similar with the structure of drawing 2 , if it removes that the pars-basilaris-ossis-occipitalis electrode 504 is formed so that a bigger surface field may be built. The one approach of forming this crown cel is forming a plug first. Sacrifice (sacrificial) The deposit of the oxide layer is carried out. the oxide layer on a plug -- a trench -- patterning -- and it etches. The vertical thing of a side attachment wall is ideal. The deposit of the pars-basilaris-ossis-occipitalis electrode material is carried out to a ** form (conformal). A pars-basilaris-ossis-occipitalis electrode material is removed from the crowning of a sacrifice oxide film for example, using chemical mechanical polishing. A sacrifice oxide layer is removed and deposition of a capacitor insulator is performed.

[0021] Drawing 6 (a) is the sectional view of the memory cell incorporating the desirable example shown by drawing 2 . This structure is formed on a substrate 600. The source 601 and a drain 603 are injected into a substrate 600. It is separated by the source and the drain and a transistor gate 605 forms both transistors. The layer insulation object 602 covers a transistor. the bit line contact 607 combines the transistor source 601 with a bit line 609 (distant (offset) from the cross section -- in order to show things, a dotted line shows). A plug 606 combines the pars-basilaris-ossis-occipitalis electrode 604 with the transistor drain 603. The obstruction object 608 and the adhesion acceleration layer 610 perform the function explained above in relation to the desirable example of drawing 2 . The pars-basilaris-ossis-occipitalis electrode 604 is covered with the capacitor insulator 612 and the top electrode 614.

[0022] Both drawing 6 (b) is the top views of one 1 transistor / 1 capacitor cel in a large number which form the memory cell array of DRAM. The sectional view shown in drawing 6 (a) shows two in 12 capacitors 650 of drawing 6 (b). A word line 652 corresponds to the transistor gate 605 of drawing 6 (a). Drawing 6 (b) shows the plug 606 of drawing 6 (a) as an element 654. The bit line contact 607 of drawing 6 (a) is an element 656 in drawing 6 (b). Drawing 7 is an example of the bottom capacitor (CUB) memory cell of a bit line of objection of the bit line top capacitor (COB) cel shown in drawing 6 (a). These structures are similar if a bit line 700 removes being formed after a capacitor 702 is formed. A bit line and the bit line plugs 704 are metals, such as a tungsten, aluminum, copper, or aluminum-Cu, typically.

[0023] Manufacture drawing 8 (a) - (c), drawing 9 (a) - (c) drawing 10 (a) - (c) and drawing 11 (a) - (c), drawing 12 (a), (b), and drawing 13 show each phase of the example of the manufacture approach of DRAM with the transverse-plane sectional view of a memory cell array.

[0024] (a) Start by the silicon substrate 800 (or SOI substrate) which has a twin well to the shallow trench segregant 802, a CMOS circumference circuit, and a memory cell array. Threshold adjustment impregnation (these may differ with a cel transistor and various circumference transistors) is performed, and the gate insulator 804 is formed. the silicification which covers a polish recon gate ingredient and a diacid-ized silicon layer -- the deposit of the tungsten is carried out, patterning of these layers is carried out after that, and the gate 806 whose crowning is an oxide film, and a circumference transistor gate and a gate level interconnect object are formed. Refer to drawing 8 (a).

[0025] (b) Pour in the drain doped lightly and form the side-attachment-wall insulator 808 on the gate by the deposit and anisotropic etching after that. By performing impurity addition, the source 810 and the drain 812 containing the circumference source / drain are formed, and the level of a transistor is completed. This structure is covered with the insulator layer 814 (for example, BPSG (borophosphosilicate glass)) by which flattening was carried out. Refer to drawing 8 (b).

[0026] (c) Appoint the hole (beer) where even the source 812 reaches into the insulator by which flattening was carried out by the photolithography, and etch it. The blanket deposit and the etching back of the polish recon by which the in SAITU (inch situ) P type dope was carried out are performed, and a stem 815 is formed in a hole. The hole which reaches to a drain 810 into the insulator by which flattening was carried out is appointed by the photolithography, and is etched. the polish recon which

and was doped, and after that -- silicification -- the blanket deposit of the tungsten cap is carried out, patterning of it is carried out, and the bit line 816 connected to a drain is formed. [inn] although a dirty stop partial layer (for example, partial layer of an oxide and a nitride) may be included -- desirable -- TEOS (tetraethyloxysilane) Precursor (precursor) from -- 500nm SiO2 formed it is -- the bit line top insulator 818 by which flattening was carried out is formed. Refer to drawing 8 (c).
[0027] (d) Form capacitor are recording node contact opening in the bit line top insulator 818 by which flattening was carried out. Opening is filled up with the polish recon 820. Flattening of the polish recon is carried out and a part for an excess is removed from the front face of the bit line top insulator 818 for example, with a chemical mechanical polish technique. Refer to drawing 9 (a).
[0028] (e) Remove the polish recon 820 from opening by Mr. Fukashi of the range of about 20 to 50nm. for example, the crowning of the polish recon plug which remains using the following processes -- silicification -- a titanium layer is formed. A hydrofluoric acid is used and it is silicon surface clearance (deglaze). It carries out and the natural oxidation film is removed. The deposit of the titanium is carried out, rapid heat annealing is performed at about 725 degrees C in nitrogen-gas-atmosphere mind after that, and a reaction is caused between titanium and silicon. The titanium and Ti-N which did not react are removed.
[0029] The spatter deposit of the (Ti0.75aluminum0.25)-N is carried out, and it is filled up with the remainder of the space made by clearance of the polish recon 820, and is a wrap about the front face of the bit line top insulator 818. Flattening of the obstruction object ingredient is carried out, and it is removed from the front face of a bit line insulator with flattening techniques, such as CMP. Thereby, it has a part for the polish recon part 820 and the Ti-aluminum-N obstruction soma 822, and the plug separated by the silicide part 821 is built. Refer to drawing 9 (b). When there is an obstruction object 822, at least two advantages are offered. 1) A polish recon plug / obstruction object interface, and an electrode / obstruction object interface are protected from the oxidizing atmosphere which exists for example, all over BST deposition. 2) Also in the case of important RISOGURAFIKKU incorrect adjustment which is things, a polish recon plug is protected with an anti-oxidation obstruction object after pars-basilaris-ossis-occipitalis electrode patterning at small geometry.
[0030] (f) Carry out the deposit of the pars-basilaris-ossis-occipitalis electrode layer 826 of 350nm platinum for the thin adhesion acceleration layer 824 (about 3nm) of Ti0.75aluminum0.25-N after that, and cover the structure. Both layers can be formed in spatter deposition. Refer to drawing 9 (c).
[0031] (g) Carry out the deposit of about 20nm hard surface mask blank layer 828 of Ti-aluminum-N, and cover the pars-basilaris-ossis-occipitalis electrode layer 826. For example, the deposit of the antireflection-film (ARC) layer 829 which consists of Si-O-N or an organic layer is carried out. The deposit of the photoresist 830 is carried out, it carries out patterning, and a pars-basilaris-ossis-occipitalis electrode is formed. Refer to drawing 10 (a). For the alternative example of a hard surface mask blank ingredient, Ti-N, Ta-N, Ta-aluminum-N, Ti-Si-N, W-Si-N, Ru-N, W-N, Ru-aluminum-N, Ru-Si-N, Cr-N, Cr-aluminum-N, Mo-N, Mo-aluminum-N, Mo-Si-N, V-N, V-Si-N, V-aluminum-N, Hf-N, Hf-aluminum-N, a 3 yuan nitride (or further pluralism) (for example, Ta-Si-N) The alloy of Ta-B-N, Ti-B-N, Zr-N, Y-N, Sc-N, La-N, aluminum-N, doped aluminum-N, Mg-N, calcium-N, Sr-N, Ba-N, and **** and Ti-N, Ga-N, nickel-N, Co-N, Ta-N, and W-N are contained. The above-mentioned all except nitrogen, for example, Ti, V-aluminum, etc. are contained in the class of alternative of a hard surface mask blank ingredient. A noble-metals insulating material alloy, for example, Pt-Si-N, Pd-Si-O, Pd-B-(O, N), Pd-aluminum-N, Ru-Si- (O, N), Ir-Si-O, Re-Si-N, Rh-aluminum-O, Au-Si-N, and Ag-Si-N are contained in another alternative example of a hard surface mask blank ingredient. Notice a hard surface mask blank layer about that the combination of the multiplex layer of another ingredient or an above-mentioned ingredient may be included.
[0032] (h) Remove comparatively the parts of the hard surface mask blank layer 828 which remains without being covered with a photoresist 830, and the ARC layer 829 using the plasma of high voltage, low bias, and the chlorine base. This etching is :pressure 6.0mTorr which is a electron cyclotron resonance plasma etching system, for example, is performed on condition that the following, source power 1500W, RF bias power 300W, and Cl2. Rate-of-flow 50sccm, Ar rate-of-flow 10sccm. Please

refer to a table 1 about the alternative example of etching conditions. Then, 830 is a photoresistO2. Ashing is carried out with the plasma and an ARC layer is removed (the ARC layer 829 may be left behind as a part of hard surface mask blank). By clearance of a photoresist and ARC, the hard surface mask blank pattern 832 is left behind on the pars-basilaris-ossis-occipitalis electrode layer 826. Refer to drawing 10 (b).

[0033]

[A table 1]

Recipe #	エッチング剤 気体流量；圧力；ECR/RF電力	Pt E/R (A/min)	TiAlN E/R (A/min)	Pt: TiAlN 選択比
1	Cl2. 50sccm:1mT:1500/900W	840	2422	1:2.9
2	Cl2/O2. 47/3sccm:1mT:1500/900W	-800	2234	1:2.8
3	Cl2/O2. 25/25sccm:1mT:1500/900W	600	88	6.8:1
4	Ar/O2. 40/10sccm:2mT:1500/900W	1715	146	12:1
5	Ar/O2. 25/25sccm:1mT:1500/900W	1700	133	13:1
6	Cl2. 50sccm:2mT:1500/300W	<100	3851	<1:38
7	Cl2. 50sccm:6mT:1500/300W	<100	3556	<1:36
8	Cl2/Ar. 50/10sccm:6mT:1500/300W	<100	3497	<1:35

[0034] (i) It is the part of the pars-basilaris-ossis-occipitalis electrode layer 826 which is not covered with the hard surface mask blank pattern 832 comparatively Ar/O2 of low voltage and high bias, Cl2 / O2 Or Ar/O2 / Cl2 It removes with the high density plasma and the pars-basilaris-ossis-occipitalis electrode 834 is formed. Etching of a platinum pars-basilaris-ossis-occipitalis electrode is :pressure 2.0mTorr accomplished on condition that the following, source power 1500W, RF bias power 900W, Ar rate-of-flow 40sccm, and O2. Rate-of-flow 10sccm. This electrode etching stops on the Ti-aluminum-N adhesion acceleration layer 824. According to this process, a pars-basilaris-ossis-occipitalis electrode without a fence is made, and careful washing after dirty is not needed.

[0035] (j) Remove the Ti-aluminum-N adhesion acceleration layer 824 from the field which remains without being covered with the pars-basilaris-ossis-occipitalis electrode 834 and a hard surface mask blank 832. Etching of a layer 824 is :pressure 6.0mTorr performed on condition that the following, source power 1500W, RF bias power 300W, and Cl2. Rate-of-flow 50sccm, Ar rate-of-flow 10sccm. Then, over-etching is performed on the same conditions. Although over-etching is not shown in drawing 11 (a), it may be prolonged in a layer insulation object or the bit line top insulator 818. This over-etching can serve as an advantage in that the capacitor insulator (for example, BST) supplied continuously can cover to homogeneity further rather than the pars-basilaris-ossis-occipitalis electrode 834 and the case where over-etching is not performed especially near the pars basilaris ossis occipitalis of an electrode. Few [more] things have theorized the defect by the stress which the structure which has the BST (that is, to be filled up with corner is not demanded) layer which continues up to insulator 818 interface by Ti-aluminum-N824 receives.

[0036] (k) Use techniques, such as RF magnetron sputtering, and it is Ba0.5 Sr0.5 TiO3 at about 500 degrees C. The deposit of about 40nm capacitor insulator layer 836 is carried out. Then, the deposit of the top electrode field plate 838 of about 100nm platinum is carried out. Refer to drawing 11 (b).

[0037] (l) Carry out the deposit of a coat and the hard surface mask blank layer 840 of (Ti0.75aluminum0.25)-N with a thickness of about 25nm on the top electrode 838 of platinum. For example, the deposit of the ARC layer 841 which consists of Si-O-N or an organic layer is carried out. The deposit of the photoresist 840 is carried out, it carries out patterning, and the boundary of a top electrode field plate is defined. Refer to drawing 11 (c).
[0038] (m) Remove comparatively the part with which the Ti-aluminum-N layer 840 is not covered using the plasma of high voltage, low bias, and the chlorine base. This etching is :pressure 6.0mTorr performed on condition that the following, source power 1500W, RF bias power 300W, and Cl2. Rate-of-flow 50sccm, Ar rate-of-flow 10sccm. A photoresist 842 and the ARC layer 841 are removed (the ARC layer 841 may be left behind as a hard surface mask blank). Then, it is the part to which BST836 in the top electrode field plate 838 and the bottom was exposed comparatively, using Ti-aluminum-N which remains as a hard surface mask blank Ar/O2 of low voltage and high bias, Cl2 / O2 Or Ar/O2 / Cl2 It removes using the plasma. This etching is :pressure 2.0mTorr performed on condition that the following, source power 1500W, RF bias power 900W, Ar rate-of-flow 40sccm, and O2. Rate-of-flow 10sccm. Refer to drawing 12 (a). A Ti-aluminum-N layer offers at least three functions. 1) Function as a hard surface mask blank of etching of the top electrode layer which is downward, and cover and enclose the top electrode field plate 838 of 2 platinum (except for the exposed edge), and at a consecutive process process, make it not polluted with platinum and a process unit functions as a dirty stop layer in formation of the beer contact between the metal layer on three, and a top electrode field plate.
[0039] (n) Carry out the deposit of the layer insulation object (for example, PETEOS) with a thickness of 500nm on the cel array 844 and the array periphery 846. Layer insulation object etching chemical, for example, Ar/CF4 / CHF3, It uses and beer 848 is etched to a field plate crowning and the circumference transistor 850. The deposit of the metals, such as liner (liner) (for example, Ti or TiN) and a tungsten, and aluminum, is carried out, it is filled up with beer 848, and the 1st metal layer 852 is formed. Refer to drawing 12 (b). The section of the below-mentioned "beer dirty stop layer" describes a substitute ingredient and a substitute etching process.
[0040] (o) The advantage of a beer [which was used for the process (n)] dirty [the consecutive metal layer 854, for example, the 2nd metal layer, and the 3rd metal layer 856] stop can be acquired. For example, the 1st metal layer 852 can be etched using the Ti-aluminum-N hard surface mask blank 853 which functions also as a beer dirty stop from the 2nd metal layer 854. The 2nd metal layer can be used for the Ti-aluminum-N hard surface mask blank 855 used in order to form the 2nd metal layer 854 as an effective dirty stop of the beer combined with the 3rd metal layer.
[0041] Drawing 14 (a) - (d) and drawing 15 (a) - (c) and drawing 16 (a), and (b) show the desirable example process for manufacturing the memory cell of the bottom capacitor of a bit line. It starts with the transistor formed like an above-mentioned process. The insulator layer 900 by which flattening was carried out is formed on the structure. (from for example, a TEOS precursor)
[0042] (a) Set even the source 902 to photolithographic one and it etches a hole (beer) into the insulator by which flattening was carried out. Refer to drawing 14 (a).
(b) Perform a blanket deposit and the etching back to the polish recon by which the in SAITU P type dope was carried out, and form a stem 904 in a hole. Refer to drawing 14 (b).
[0043] (c) silicification -- form the titanium layer 906 in the crowning of a polish recon plug using the following processes. Silicon surface clearance is performed using a hydrofluoric acid, and the natural oxidation film is removed. The deposit of the titanium is carried out, rapid heat annealing is performed at about 725 degrees C in nitrogen-gas-atmosphere mind after that, and a reaction is caused between titanium and silicon. The titanium and Ti-N which did not react are removed. Refer to drawing 14 (c).
[0044] (d) It is a wrap about the front face of the insulator 900 by which carried out the spatter deposit of the Ti0.75aluminum0.25-N, and was filled up with the remainder of the space made by clearance of the polish recon 904, and flattening was carried out. Flattening of the obstruction object ingredient is carried out, and it is removed from the front face of a bit line insulator with flattening techniques, such as CMP. The plug which has a part for the polish recon part 904 and the Ti-aluminum-N obstruction soma 908, and is separated by the silicide part 906 by this is built. Refer to drawing 14 (d).

[0045] (e) Carry out the deposit of the thin adhesion acceleration layer 910 (about 3nm) of Ti0.75aluminum0.25-N, then the pars-basilaris-ossis-occipitalis electrode layer 912 of 350nm platinum, and cover the structure. Both layers can be formed by the spatter deposit. The deposit of about 20nm hard surface mask blank layer of Ti-aluminum-N (not shown) is carried out, and the pars-basilaris-ossis-occipitalis electrode layer 912 is covered. For example, the deposit of the antireflection-film (ARC) layer (not shown) which has Si-O-N or an organic layer is carried out. The deposit of the photoresist (not shown) is carried out, it carries out patterning, and a pars-basilaris-ossis-occipitalis electrode is formed. The parts of the hard surface mask blank layer which remains without being covered with a photoresist, and an ARC layer are removed (an ARC layer may be left behind as a part of hard surface mask blank). The part of the pars-basilaris-ossis-occipitalis electrode layer 912 which is not covered with a hard surface mask blank pattern is removed. The Ti-aluminum-N adhesion acceleration layer 910 is removed from the field which remains without being covered with the pars-basilaris-ossis-occipitalis electrode 912. Refer to drawing 15 (a).
[0046] (f) Ba0.5 Sr0.5 TiO3 The deposit of about 40nm capacitor insulator layer 914 is carried out at about 500 degrees C using techniques, such as RF magnetron sputtering. Then, the deposit of the top electrode field plate 916 of about 100nm platinum is carried out. The deposit of a (Ti0.75aluminum0.25)-N coat and the hard surface mask blank layer 918 with a thickness of about 25nm is carried out on the top electrode 916 of platinum. For example, the deposit of the ARC layer (not shown) which consists of Si-O-N or an organic layer is carried out. The deposit of the photoresist (not shown) is carried out, it carries out patterning, and the boundary of a top electrode field plate is defined. The part with which the Ti-aluminum-N layer 918 is not covered is removed. An ARC layer and a photoresist are removed (an ARC layer may be left behind as a part of hard surface mask blank). Then, the part to which BST914 in the top electrode field plate 916 and the bottom was exposed is removed, using Ti-aluminum-N which remains as a hard surface mask blank. Refer to drawing 15 (b).
[0047] (g) On the structure, carry out the deposit of the layer insulation object 920 (for example, PETEOS) with a thickness of 500nm, and it carries out flattening. Bit line contact beer 922 is etched to the drain 924 of a transistor. Refer to drawing 16 (a).
[0048] (h) the silicification which carried out the deposit of the titanium and was mentioned above at the process (c) -- form a silicide (not shown) in the transistor drain 924 using a process. desirable -- SiO2 it is -- in order to remove the insulator by which carried out the deposit of the thin contact hole liner 923 according to the ** form (conformal) CVD process, and the deposit was carried out on the drain of a transistor, flattening etching continues. Refer to drawing 16 (a).
[0049] (i) The deposit of the bit line conductors 926, such as a tungsten or polish recon in contact with a drain 924, is carried out, and a bit line is formed. Refer to drawing 16 (b). Etching of an etching process platinum electrode is the process which should tackle the boldest in a process. The platinum, its oxide film, and platinum halogenated compound as noble metals have dramatically low volatility altogether at a moderate temperature which is used in a dry etching process. A platinum etching process is physical etching which mainly faces chemically. Consequently, an etch rate becomes slow, the etch selectivity to resistance, and an oxide film/nitride becomes low, and a temporary side-attachment-wall fence is formed in a still more important thing as a result of the re-deposition of the platinum under etching. It means that the costs of a resist become large that a platinum etch rate is slow and the etch selectivity to resistance, and an oxide film/nitride is low (since it is etched more quickly than the ingredient which is downward, a thick resist layer is needed).
[0050] A hundreds of nanometers oxidization (or nitriding) silicon layer can be used as a hard surface mask blank of pars-basilaris-ossis-occipitalis electrode etching of platinum. Pt:SiO2 Or Pt:SiNx A selection ratio is from 2 to 3 typically. Since the selection ratio between field oxide and a hard surface mask blank is small, clearance of the hard surface mask blank by dry cleaning or the wet etching process after following Pt etching can serve as too much field oxide loss. SiO2 And SiNx Dry etching is performed by the etching chemical of the fluorine base. Since it is not desirable to use both a fluorine and chlorine etching within the same etching chamber, platinum etching of the chlorine base of a fluorine process is conflicting. For this reason, the hard surface mask blank ingredient which can be

removed by etching of the chlorine base is desirable.
[0051] Ti-aluminum-N is alternative desirable as a hard surface mask blank ingredient of a platinum electrode in several reasons. Ti-aluminum-N is easily etched [1st] with comparatively low bias power (the etching agent used in order to obtain the data of a table 1 -- about 500 -- smaller than W) within the chlorine content plasma (Cl2, Cl2 / Ar, or Cl2/O2 containing O2 [little (for example, fewer than about 15%)]). For this reason, it is easy to distinguish from the platinum typically removed with high bias power. The etching compound which contains [2nd] oxygen, for example, O2 [high], Ar/O2 which has concentration The plasma, Ar/O2 / Cl2 Or Cl2 / O2 Within the plasma, Ti-aluminum-N is etched very slowly. As a matter of fact, it depends for the validity as a hard surface mask blank layer of Ti-aluminum-N on the oxygen in the etching chemical combined with the aluminum of a hard surface mask blank layer in order to form the aluminum oxide which functions as a self-passivation layer of a hard surface mask blank. Therefore, a desirable hard surface mask blank ingredient contains at least 1% of aluminum. Notice the upper limit of the concentration of the aluminum of Ti-aluminum-N about being applied to the hard surface mask blank layer which remains on the structure as a conductive element like the beer dirty stop layer explained below. Please refer to the process (g) of an above-mentioned example process about a substitute hard surface mask blank ingredient.
[0052] The same logic is applied also to the adhesion acceleration layer of an above-mentioned example used in order to stop platinum etching so that a dirty stop layer, for example, the layer insulation object which is downward, may not be reached. In addition to generally protecting a layer insulation object, the adhesion acceleration layer explained by **** also decreases minute trenching in the base of a platinum electrode produced with the ion reflected from the inclined side attachment wall. This is useful also to avoiding the plug loss in the incorrect adjustment between the Pori plug and a pars-basilaris-ossis-occipitalis electrode.
[0053] In the beer dirty stop layer latest device, in some DRAM applications for which 500nm or more of depth of the beer to a circumference transistor may differ even from a capacitor top electrode field plate especially since the size of beer is small and the aspect ratio of beer is enlarged, in order to form beer, a long over etching process may be used. Although TiN is used as the beer dirty stop on the interconnect conductor of a memory cell, or a top electrode, and an ARC layer, the etch selectivity to an oxide film is only 30:1. Such a selection ratio is not enough for long over etching and the thin ARC layer which a desirable thing also has.
[0054] It turns out that the alternative example of TiN offers the outstanding etch selectivity to both an oxide film and a nitride. The layers 840, 853, and 855 of an example explained by **** may be 1 Ti-aluminum, Ti-aluminum-N, Ta-aluminum, aluminum-N or 2 Ti-aluminum/Ti-N, Ti-aluminum-N/Ti-N, Ta-aluminum/Ti-N, Ti-aluminum/Ti-aluminum-N and other same combination (even if Ti-N is included, it is not necessary to contain) that forms two-layer, or above-mentioned combination which forms 33 layer. A desirable ingredient is (Ti1-x Alx)-N, x is aluminum concentration and the range of it is about 0.01 to 0.60 here. The upper limit of an aluminum content is mainly decided by the conductivity of an ingredient (in Ti-aluminum-N, resistance of an ingredient increases with an aluminum content). As for a beer dirty stop ingredient, it is desirable for it to have high conductivity in order to form contact between the conductors (for example, top electrode 838 of drawing 12 (b)) and upside conductors (for example, 1st metal layer 852 of drawing 12 (b)) which are downward. The minimum aluminum concentration is decided according to the need of forming sufficient self-inactivation aluminum oxide layer mainly raising etch selectivity, and the need for oxidation resistance in case a dirty stop layer covers the top electrode of a memory cell capacitor with a special case.
[0055] Ar/CF4 / CHF3 The following etch selectivity is obtained by using an etching chemical. Oxide film: For TiN, 28.4:1 and oxide-film:Ti0.75aluminum0.25N are 48.2:1 and oxide-film:TiAl3. 228:1. The etching conditions are as follows. Pressure 250mTorr, RF bias power 800W, Ar rate-of-flow 200sccm, and CF4 Rate-of-flow 70sccm and CHF3 Rate-of-flow 35sccm. The same result is Ar/CF4 / O2. It is obtained by nitride etching using an etching chemical. The selection ratio of a nitride is as follows. Nitride: For TiN, 12.9:1 and nitride:Ti0.75aluminum0.25N are 30.3:1 and nitride:TiAl3. 39.5:1. silicification -- silicon etching -- Ar/CF4 / O2 :pressure 250mTorr performed using the conditions of the

following [etching], RF bias power 800W, Ar rate-of-flow 200sccm, and CF4 Rate-of-flow 70sccm and O2 Rate-of-flow 25sccm. Note that the same etch selectivity is expectable by the high density plasma etching agent. A substitute etching chemical is CF4, CHF3, CH two F2, CH3 F, O2, Ar, SF6, C two F6, C four F8, and C three F6. And other fluoride or a par full ORINE Ted (perfluorinated) hydrocarbon may be included. At least one can use one or the gas beyond it which is the fluorine base.
[0056] By using an above-mentioned ingredient, the oxide film etch selectivity to a beer dirty stop layer increases, and still longer over etching becomes possible, without making the hole which passes along a beer dirty stop layer (for example, layer 840 of drawing 12 (b)) by that cause. In the application of DRAM, if the oxide film etch selectivity to an electrode is still higher, fear [exhausting / the electrode of a beer pars basilaris ossis occipitalis] will decrease. Such consumption may make contact resistance or a device defect increase. It is the reflexibility (reflectance) which gives the thickness of a layer at a metal patterning process when two-layer or a three-tiered structure is used. It optimizes so that it may become still smaller. As mentioned above, the same advantage may be attained when etching to such a beer dirty stop layer through silicon nitride.
[0057] Notice a beer dirty stop and hard surface mask blank configuration of an above-mentioned ingredient about that it may be applied to devices other than a memory circuit. In the situation of the arbitration actually connected to the layer which one layer (for example, metal layer) adjoins, an above-mentioned beer dirty stop ingredient can be used. The above-mentioned ingredient is especially effective, when [when combined with the layer in the bottom in a different distance from the layer which has one layer upwards through beer therefore] the long over etching of beer is needed so that the time amount which makes deeper beer may be given. For example, a microprocessor, a digital signal processor, a memory circuit, etc. can acquire the advantage of such a dirty stop layer also with what kind of semiconductor device substantially.
[0058] Although this invention was explained with reference to the example for instantiation, it does not have the intention of this explanation being interpreted by restrictive semantics. Various deformation of the example for these instantiation, and not only combination but other examples of this invention are also clear to this contractor, if this explanation is referred to. For example, the memory circuit of an example explained here may be embedded at the integrated circuit which has a microprocessor or a processor like a digital signal processor. Therefore, an attached claim means including all these deformation and combination.
[0059] The following term is further indicated about the above explanation.
(1) The pars-basilaris-ossis-occipitalis electrode which is a memory circuit containing a memory cell and has a conductive adhesion acceleration layer on the (a) 1st front face, The capacitor which has a top electrode in contact with the accumulation layer in contact with the 2nd front face of said pars-basilaris-ossis-occipitalis electrode, and said accumulation layer, (b) The transistor containing the 1st and 2nd terminals and word line control terminals and the bit line combined with the transistor terminal of the (c) above 1st are included. Said pars-basilaris-ossis-occipitalis electrode It is combined with said 2nd transistor terminal by the plug including the obstruction object which adjoins said adhesion acceleration layer, and said obstruction object is a memory circuit thicker than said adhesion acceleration layer.
[0060] (2) It is the memory circuit in which it is a memory circuit given in the 1st term, and said obstruction object contains Ti-aluminum-N.
(3) It is the memory circuit in which it is a memory circuit given in the 1st term, and said contact acceleration layer contains Ti-aluminum-N.
(4) It is the memory circuit in which it is the memory circuit of a publication of the 2nd term or the 3rd term, and said Ti-aluminum-N contains the aluminum of 0 to 50% of range.
(5) It is the memory circuit said whose Ti-aluminum-N it is a memory circuit given in the 4th term, and is (Ti0.75aluminum0.25)-N.
(6) It is the memory circuit said whose pars-basilaris-ossis-occipitalis electrode it is a memory circuit given in the 1st term, and is platinum.
[0061] (7) It is the approach of etching the configuration of the platinum layer on said 2nd ingredient, without etching the 2nd ingredient substantially. (a) An adhesion acceleration layer is formed between

said platinum layer and said 2nd ingredient. (b) A hard surface mask blank layer is formed on said platinum layer (c). Said configuration of a desired dimension is followed. Patterning of said hard surface mask blank layer is carried out, and it is etched (d). It is the approach of etching the part of said platinum layer which is not covered with said hard surface mask blank layer, and including the process which suspends said etching on said adhesion acceleration layer.
[0062] (8) It is an approach including being an approach given in the 7th term and a process (a) forming a Ti-aluminum-N layer between said platinum layer and a diacid-ized silicon layer.
(9) It is an approach including being an approach given in the 7th term and a process (b) forming a Ti-aluminum-N layer on said platinum layer.
(10) It is the approach are an approach given in the 8th term or the 9th term, and said Ti-aluminum-N layer contains at least 1% of aluminum.
(11) It is an approach including being an approach given in the 7th term and a process (c) etching said hard surface mask blank layer by the chlorine content etching agent.
(12) It is an approach including being an approach given in the 7th term and a process (d) etching said some of platinum by the oxygen content etching agent.
[0063] (13) It is the approach of etching platinum (a). A Ti-aluminum-N hard surface mask blank layer is formed on said platinum (b). Patterning of said Ti-aluminum-N hard surface mask blank layer is carried out, it etches by the chlorine content etching agent, and a desired pattern is formed (c). Approach including the process which etches said platinum by the oxygen content etching agent.
[0064] (14) an approach given in the 13th term -- it is -- said chlorine content etching agent -- Cl2, Cl2 /2 / O2 from -- approach chosen from the group who changes. [Ar and Cl2]
(15) an approach given in the 13th term -- it is -- said oxygen content etching agent -- Ar/O2, Cl2 / O2 from -- approach chosen from the group who changes.
(16) an approach given in the 14th term -- it is -- said chlorine content etching agent -- Cl2 / O2 it is -- approach with few amounts of content oxygen than said oxygen content etching agent.
(17) It is the approach of being an approach given in the 13th term and accomplishing said etching of a process (b) with a plasma etching system with bias power still lower than said etching of a process (c).
[0065] (18) It is the high beer etching process of a selection ratio (a). The dirty stop layer of the ingredient chosen from the group who consists of Ti-aluminum, Ti-aluminum-N, Ta-aluminum, aluminum-N, Ti-aluminum/Ti-N, Ti-aluminum-N/Ti-N, Ta-aluminum/Ti-N, and Ti-aluminum/Ti-aluminum-N is formed (b). An insulator layer is formed on said dirty stop layer (c). Process including the process which etches said insulator layer by the fluorine content etching agent.
 [0066] (19) It is the approach it is an approach given in the 18th term, and said ingredient is Ti-aluminum-N.
(20) It is the approach it is an approach given in the 19th term, said Ti-aluminum-N is (Ti1-xAlx)-N, and the range of x is about 0.01 to 0.60 here.
(21) It is the approach it is an approach given in the 18th term, and said ingredient is Ti-aluminum.
(22) an approach given in the 21st term -- it is -- said ingredient -- TiAl3 it is -- approach.
(23) an approach given in the 18th term -- it is -- said insulator layer -- diacid-ized silicon -- it is -- said fluorine content etching agent -- Ar/CF4 / CHF3 it is -- approach.
(24) an approach given in the 18th term -- it is -- said insulator layer -- a silicon nitride -- it is -- said fluorine content etching agent -- Ar/CF4 / O2 it is -- approach.
[0067] (25) The electrode structure for a capacitor. The adhesion acceleration section contacts the oxidation obstruction object of a contact plug including the pars-basilaris-ossis-occipitalis electrode containing the contact plug in which this electrode structure includes the oxidation obstruction object 208, and the conductive adhesion acceleration section 210 and the oxidation-resistance section 204. In the further example, an oxidation obstruction object and the adhesion acceleration section contain Ti-aluminum-N.

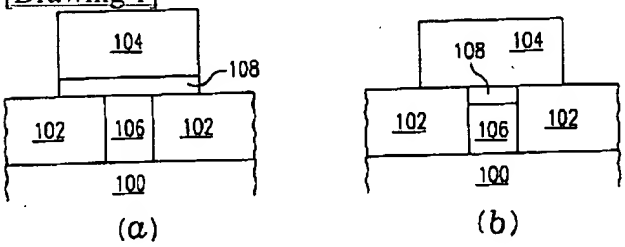
[Translation done.]

* NOTICES *

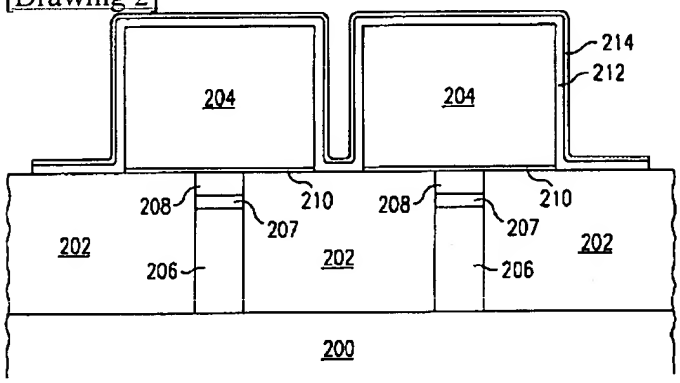
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

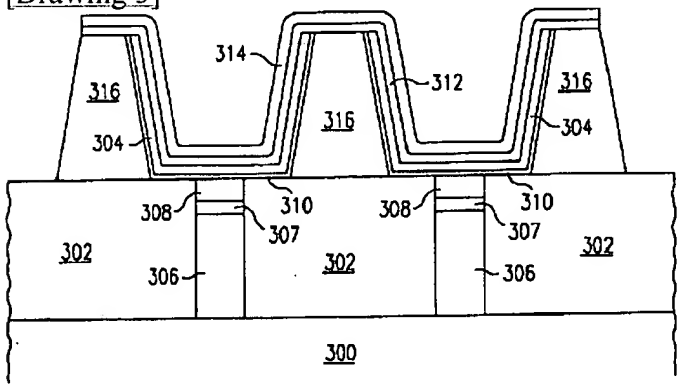
[Drawing 1]



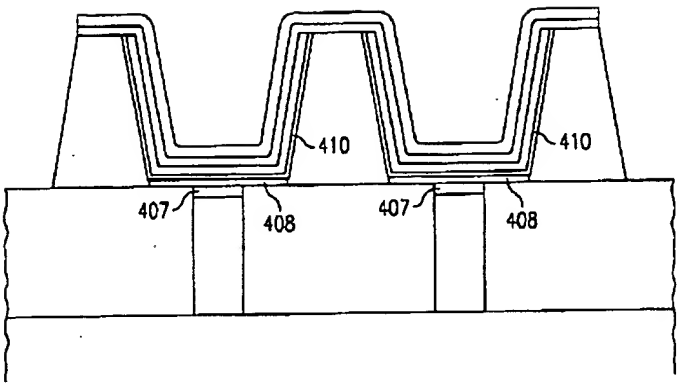
[Drawing 2]



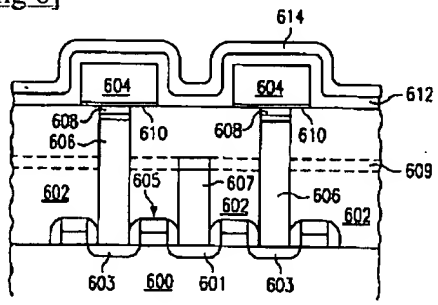
[Drawing 3]



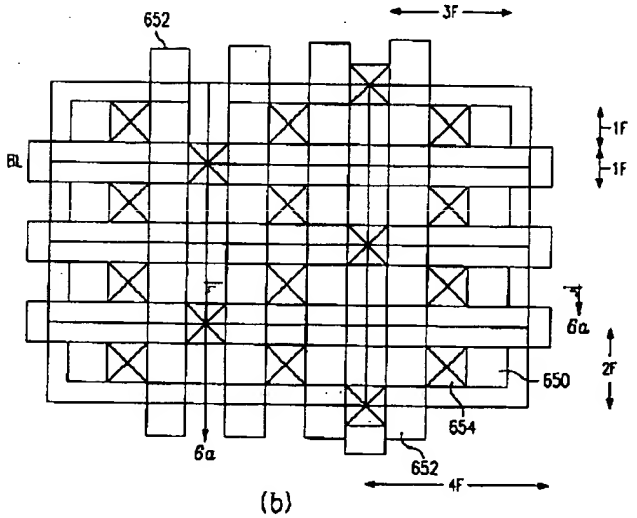
[Drawing 4]



[Drawing 6]

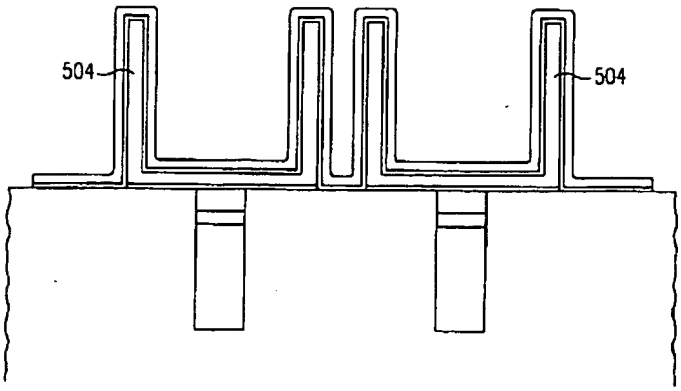


(a)

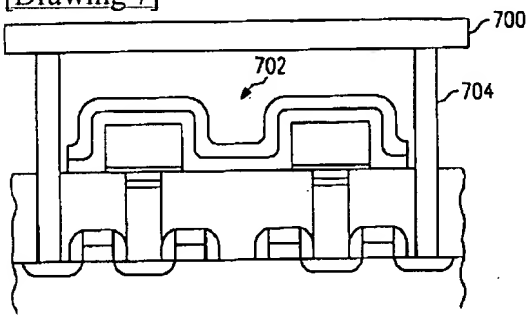


(b)

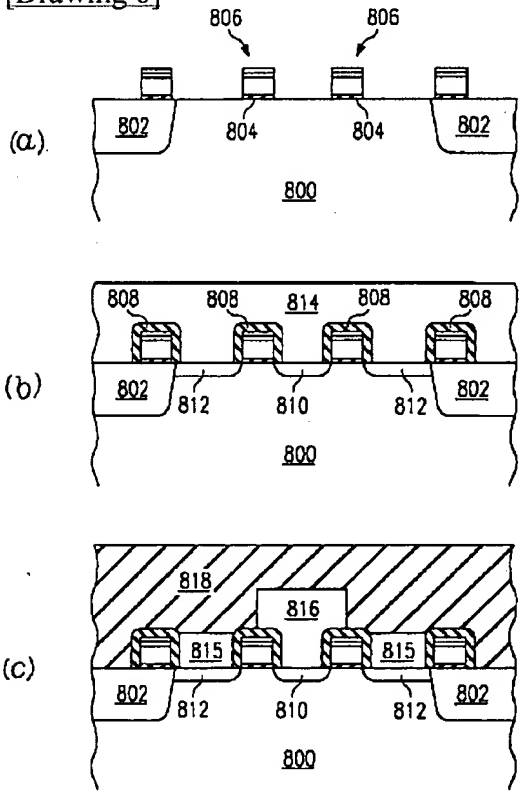
[Drawing 5]



[Drawing 7]

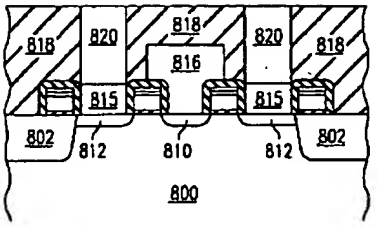


[Drawing 8]



[Drawing 9]

(a)



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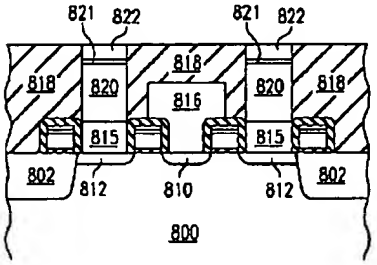
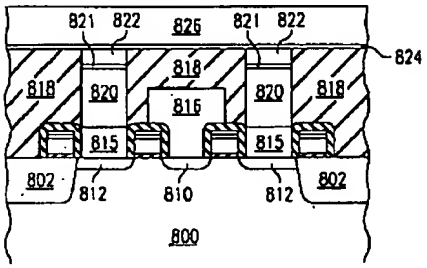
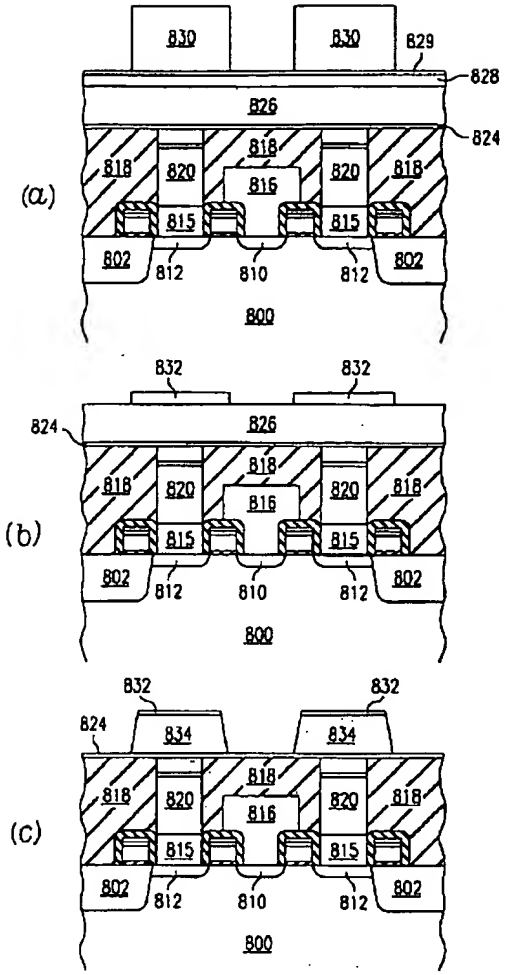


(c)



[Drawing 10]


(a)
830
830
829
828
826
824
818
820
816
820
818
815
815
802
812
810
812
802
800
(b)
832
832
824
826
818
820
816
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818
815
815
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812
810
812
802
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(c)
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834
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802
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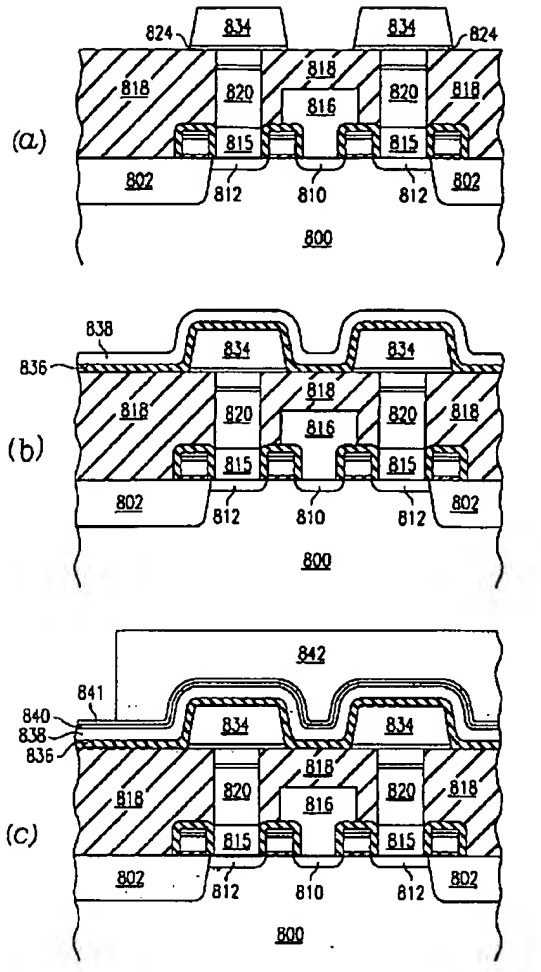
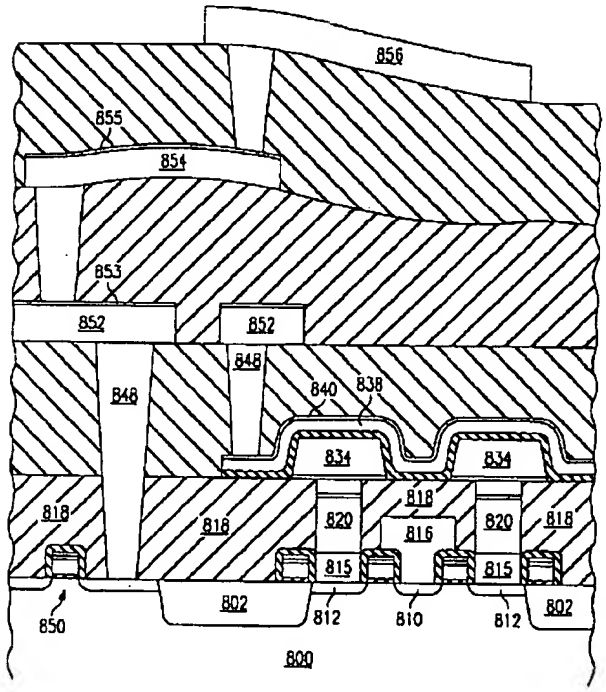
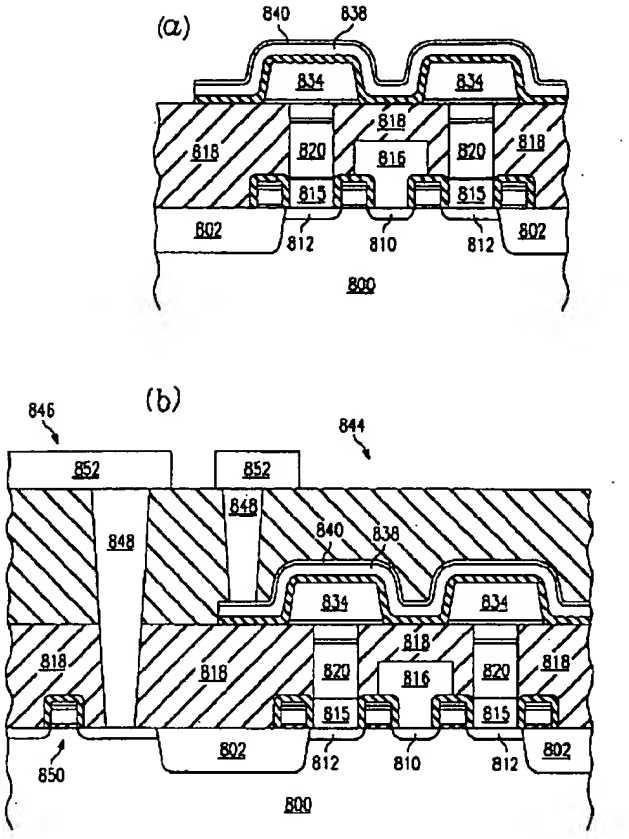
[Drawing 11]



[Drawing 13]



[Drawing 12]


(a)
840
838
834
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816
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812
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812
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800
(b)
846
844
852
852
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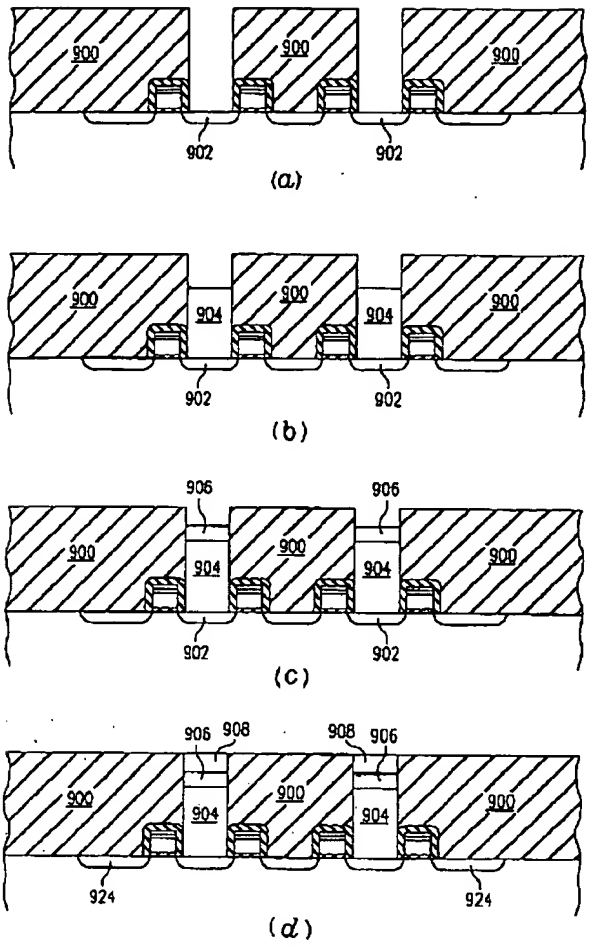
[Drawing 14]


900
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902
(a)
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904
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904
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(b)
906
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900
904
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(c)
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908
908
906
900
904
900
904
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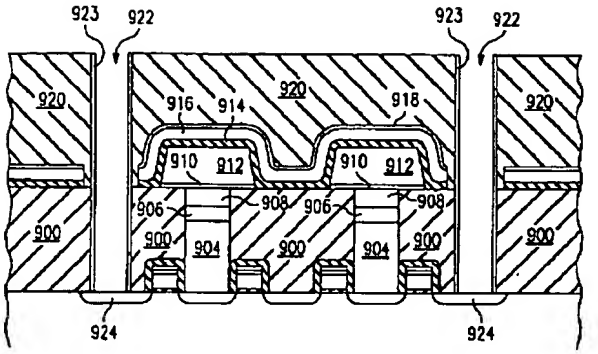
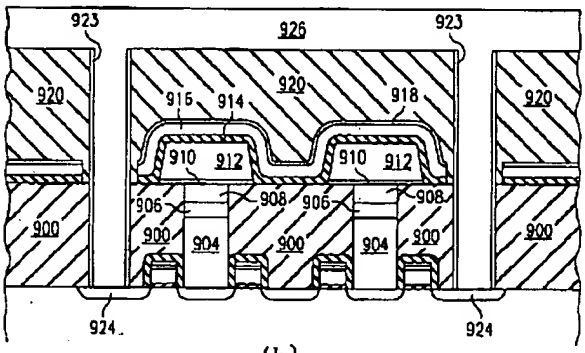
924
924
(d)

[Drawing 16]

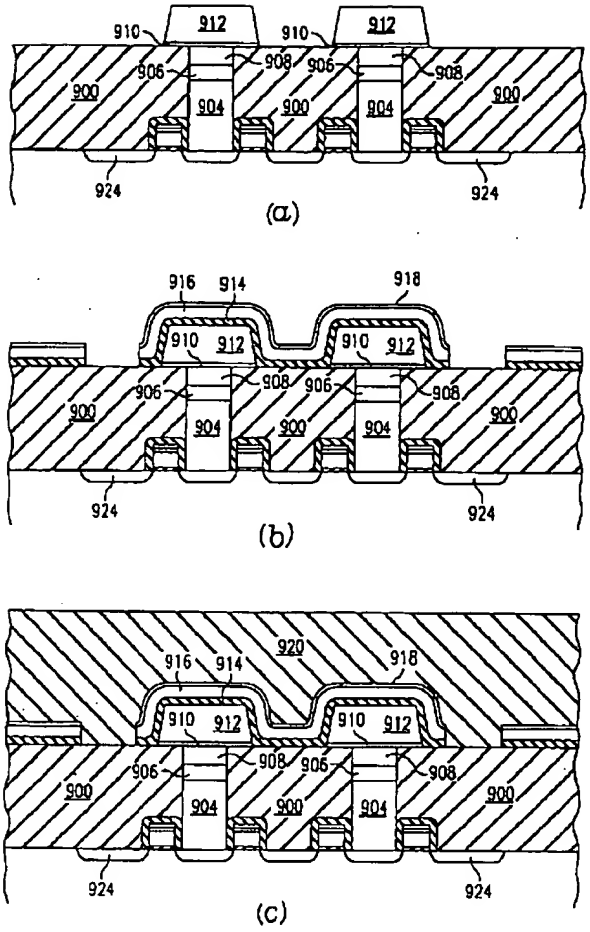


(a)



(b)

[Drawing 15]



[Translation done.]